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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,339	01/16/2004	Scott T. Becker	ARTCP043	7710

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EXAMINER	
NGUYEN, HIEP	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/759,339	BECKER ET AL.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9,10 and 26-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 9, 10 and 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy (USP. 6,271,713) in view of Wong et al. (USP. 6,137,313), Okamoto et al. (USP. 6,784,719) and Horiguchi et al. (USP. 6,504,402).

Regarding claim 1, figures 1 and 4 of Krishnamurthy shows a feed forward circuit for reducing delay through an input buffer comprising: an inverter (152), an inverting circuit (154) coupled to the inverter, a feed forward transistor (M1), wherein the feed forward transistor decreases an amount of time required for the output of the inverting circuit to change state when the input (Vin) changes from low to high (col.2, lines 58-64).

Figure 1 of Krishnamurthy does not show that the inverter is powered by a first voltage level and the transistors of the inverter have a first size; the inverting circuit comprises transistors having a second size and powered by a second power supply wherein the second voltage level is lower that the first voltage level.

Figure 1A of Okamoto shows a level shift circuit comprising an inverter (202) power by a first supply voltage (Vcc1) and an inverting circuit (203) power by a second supply voltage (Vcc2) for shifting up or down the level of the input signal depending on the level of the first and second supply voltages. If the level of the level of the second supply voltage is lower than the level of the first supply voltage, the circuit of Okamoto will shift down the input voltage for conforming to the voltage requirement of the other circuit connected to the output of the feed forward circuit. Therefore, it would have been obvious to an artisan having skills in the art to apply a second voltage, lower than the first voltage (Vdd), supplied to the inverting circuit

(154) of Krishnamurthy for shifting down the input voltage for conforming to the voltage requirement of the other circuit that is connected to the output of the feed forward circuit.

Figure 1 does not show that the feed forward transistor (M1) is smaller than the transistors of the inverter and the inverting circuit. Figure 2B of Wong shows a pull-up transistor having small size for minimizing the on current thus, reducing power consumption (col. 2, lines 26-35). Therefore, it would have been obvious to an artisan having skills in the art to use a small size pull-up transistor as taught by Wong in Krishnamurthy circuit for minimizing the on current and reducing power consumption.

Regarding claims 2-4, when input (Vin) goes high, transistor (M1) is turned on and the output (Vout) is increased. When input (Vin) goes low, transistor (M1) is turned off and the output (Vout) ceases to increase. Figure 4 of Krishnamurthy shows that the decrease in the amount of time required for the output of the inverting circuit to change state is at least one gate delay of the inverting circuit.

Regarding claim 5, the combination of Krishnamurthy and Okamoto and Wong shows that the inverting circuit comprises p-channel and n-channel transistor and the p-channel of the inverting circuit is coupled to the second voltage (Vcc2).

Regarding claim 6, the combination of Krishnamurthy, Wong et al. and Okamoto includes all the limitations of claim 6, except for the limitation that there is a high impedance transistor coupled to the n-channel transistor and ground. Figure 4 of Horiguchi shows an inverter having a high impedance transistor (MS1) coupled to the n-channel transistor and ground for having a low power consumption mode by providing a high impedance to the inverter when it is turned off (col. 7, lines 30-35). Therefore, it would have been obvious to an artisan in the art to implement a high impedance transistor taught by Horiguchi to the second transistor of the inverting circuit for having a low power consumption mode by providing a high impedance to the inverting circuit when it is turned off.

Regarding claim 9, figure 4 of Krishnamurthy shows that the feed forward transistor (M1) turns off, allowing the voltage at the output of the inverting circuit to transition to a LOW state when the input to the inverter transitions to a LOW state.

Regarding claim 10, figure 4 of Krishnamurthy shows that the inverting circuit includes an n-channel transistor and a p-channel transistor, the n-channel transistor having a first terminal coupled to ground, a gate coupled to the input of the inverting circuit, and a second terminal coupled to a first terminal of the p-channel transistor, the p-channel transistor having a gate coupled to the input of the inverting circuit.

Regarding claims 26 and 27, the combination of Krishnamurthy and Okamoto and Wong includes all the limitations of claims 26 and 27 except for the limitations of "ring voltage" and "core voltage". However, it is old and well known and it would have been an obvious matter of preference bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed relative predetermined value of a differential input voltage limitations because applicant has not disclosed that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another relative predetermined value of a differential input voltage. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III). Therefore, it would have been obvious to one having ordinary skill in the art to select the voltages (Vcc1) and (Vcc2) to be the values of "ring voltage" and "core voltage" dependent upon particular environment of

use to ensure optimum performance.

Regarding claim 28, the combination of Krishnamurthy and Okamoto and Wong shows that the "I/O ring size of transistors" (M2, M3) are larger than the "core size transistors" (116, 118).

Allowable Subject Matter

Claims 7 and 8 are objected to because the prior art of records fails to teach or suggest a feed forward circuit comprising a low impedance transistor as called for in claim 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 130272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen
08-11-05

TUAN T. LAM
PRIMARY EXAMINER